

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 10/574,030 Confirmation No. 8030
Applicant : VAN SCHAIJK, Robertus Theodorus
Filed : March 27, 2006
TC/A.U. : 2811
Examiner : HSIEH, Hsin Yi

Docket No. : **NL03 1167 US1**
Customer No. : 65913

Title : Two-Transistor Memory Cell and Method for Manufacturing

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE & AMENDMENT

Sir:

In response to the Office Action of September 18, 2009, in which a restriction requirement was made, Applicant elects to prosecute the claims of Group I, with traverse.